new correlation result is available every four clocks. Hence the correlation proceeds at a rate of 20 MHz/4=5 M points/sec. For a 3×3 correlation, the rate is 6.67 M points/sec. In a similar manner image convolution may be implemented with the DFP device.

## OTHER APPLICATIONS

The high performance and cascadability of the DFP is very attractive for implementing various functions in a radar system. In a typical radar system the DFP can implement the matched filter pulse compressor as well as various other digital filters in the system. Other applications include adaptive filters, Butterfly computations, echo cancellation, and complex multiplications.

Thus while the invention has been described with reference to a specific embodiment and specific applications the description is illustrative of the invention and not to be construed as limiting the invention. Various modifications and applications may occur to those skilled in the art without departing from the true spirit and scope of the invention as defined by the appended claims.

What is claimed is:

1. A digital filter processor comprising

a plurality of processing cells, each cell including a data register, a coefficient register, a multiplier-accumulator for processing and accumulating the contents of said data register and the contents of said coefficient register and producing an output,

means connecting said plurality of cells whereby a coefficient is serially translated to each cell for multiplying with a data word,

means for applying data in parallel to all cells, and

multiplex means connected to the outputs of said accumulators for receiving outputs from all cells, said multiplex means including a multiplexer for selectively receiving an output from each cell, an output stage for summing said outputs, said output stage including an adder for shifting and adding said outputs from said cells.

2. The digital filter processor as defined by claim 1 and including address means connected to all cells for selecting a cell output for application to said multiplexer.

3. The digital filter processor as defined by claim 2 and further including a coefficient input for receiving coefficients for application to said plurality of cells serially, and a coefficient output for transmitting coefficients after application to all of said cells, whereby a plurality of said digital filter processors can be concatenated to increase the number of coefficients for multiplication with data.

4. A digital filter processor comprising

a plurality of processing cells, each cell including a data register, a coefficient register, a multiplier-accumulator for processing and accumulating the contents of said data register and the contents of said coefficient register and producing an output, said multiplier/accumulator including a multiplier for receiving and multiplying the contents of said data register and the contents of said coefficient register and producing an output, a first adder having a first and second inputs and an output, means connecting the output of said multiplier to said first input, a first accumulator having an input connected to said output of said adder and having an output connected to said second input,

means connecting said plurality of cells whereby a coefficient is serially translated to each cell for multiplying with a data word,

means for applying data in parallel to all cells,

multiplex means connected to the outputs of said accumulators for receiving outputs from all cells, and

an output stage for summing said outputs.

5. The digital filter as defined by claim 4 wherein said multiplex means includes a multiplexer for selectively receiving an output from each cell, and a second adder and a second accumulator for shifting, adding and accumulating outputs from all cells.

6. The digital filter as defined by claim 5 and including address means connected to all cells for selecting a cell output for application to said multiplexer.

7. The digital filter as defined by claim 6 and further including a coefficient input for receiving coefficients for application to said plurality of cells serially, and a coefficient output for transmitting coefficients after application to all of said cells, whereby a plurality of said digital filter processors can be concatenated to increase the number of coefficients for multiplication with data.

8. The digital filter processor as defined by claim 7 wherein each cell includes a plurality of registers and at least one multiplier serially connected with said coefficient register whereby a coefficient of one cell can be selectively delayed before being passed to an adjacent cell for sample rate reduction.

9. A method of filter processing of digital data using a finite impulse response defined by a plurality of coefficients comprising the steps of

providing a plurality of multiplier/accumulator cells,

providing data words in parallel to all cells in sequence,

providing coefficients serially to all cells in sequence including optionally delaying said coefficients between cells for sample rate reduction,

multiplying a data word by coefficients in each cell to obtain products, and

optionally accumulating the products from selected cells including selectively shifting the product of a cell and adding the shifted product to the product from another cell.

10. The method as defined by claim 9 wherein said data words and said coefficients include sign mode bits.

11. The method as defined by claim 9 wherein said step of optionally accumulating the products is not exercised and products from said selected cells are provided as filter outputs.

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